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TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. BUR920040134US1

Re Application Of: **Paul H. Bergeron et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/711,978	10/18/2004	Unassigned	044152	Unassigned	Unassigned

Title: **IMPROVING SYSTEMATIC YIELD IN SEMICONDUCTOR MANUFACTURE**

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☐ the fee set forth in 37 CFR 1.17(p).

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Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

☐ A check in the amount of is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below.

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C. MUELLER

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Dated: 11/10/04

Richard M. Kotulak, Reg. 27712
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cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Paul H. Bergeron, et al.

Docket No.: BUR920040134US1

Serial No.: ~~Unassigned~~ 10/711,978

Group Art Unit: Unassigned

Filed: ~~Concurrently~~ 10/18/2004

Examiner: Unassigned

For: **IMPROVING SYSTEMATIC YIELD IN SEMICONDUCTOR MANUFACTURE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. A copy of the non-US patent documents is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Respectfully submitted,

Andrew M. Calderon
Reg. No. 38,093

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Form PTO-1449 (Modified)	Attorney Docket No.: BUR920040134US1	Serial No: Unassigned
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: Paul H. Bergeron, et al.	
(Use several sheets if necessary) NOV 1 2 2004 Page 1 of 1	Filing Date: Concurrently	Group: Unassigned

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
							☐	☐

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

			R.L. Hunt, et al., "Automatically Rerouting Wires on Printed-Circuit Boards to Avoid Noise Coupling Problems", IBM Technical Disclosure Bulletin, Vol. 18, No. 3, August 1975, p. 762-766.
			J.Z. Su, et al., "Post-Route Optimization for Improved Yield Using a Rubber-Band Wiring Model", Computer Aided Design, 1997. Digest of Technical Papers., 1997. IEEE/ACM International Conference on Nov. 9-13, 1997, p. 700-706.
			R. Prasad, et al., "The Effect of Placement on Yield for Standard Cell Designs", url = "citeseer.ist.psu.edu/380923.html"
			A.B. Kahng, et al., "Non-Tree Routing for Reliability and Yield Improvement", Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on Nov. 10-14, 2002, p. 260-266.
			A. Venkataraman, et al., "Determination of Yield Bounds Prior to Routing", Defect and Fault Tolerance in VLSI Systems, 1999. DFT '99. International Symposium on Nov. 1999, p. 4-13.
			P. Kudva, et al., "Measurements for Structural Logic Synthesis", Computer Aided Design of Integrated Circuits and Systems, IEEE Transactions on Vol. 22, Iss. 6, June 2003, p. 665-674.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.